5. (Twice Amended) A semiconductor testing method for testing semiconductor devices, comprising:

reading measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, including a test vector data and data of good samples and faulty samples returned to a manufacturer;

supplying the test vectors to the good samples and the faulty samples;

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

applying test vectors of the effective address pairs to the semiconductor devices for testing.

9. (Twice Amended) A program with which a semiconductor testing method for testing semiconductor devices is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, the program comprising:

instructions configured to read measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer;

instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

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B2 Cont'd

instructions configured to apply test vectors of the effective address pairs for testing.

B3 Sub C

13. (Twice Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, comprising:

reading measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

supplying test vector data to good and faulty samples;

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

applying test vectors of the effective address pairs to a semiconductor device; and

specifying a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

B4 Sub C Cont'd

16. (Twice Amended) A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, comprising:

a read circuit configured to read measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein

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the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

a determination circuit configured to supply the test vector data to the good samples and faulty samples, and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply test vectors of the effective address pairs to a semiconductor device and to specify a faulty part by measuring an emission from the semiconductor device.

19. (Twice Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, the program comprising:

instructions configured to read measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

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